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PATENT
Docket No. P1296

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): BIN YU

SERIAL NO.: 09/826,472 EXAMINER: RON E. POMPEY

FILED: APRIL 4, 2001 ART UNIT: 2812

TITLE: METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A NITRIDE/HIGH-K/NITRIDE GATE DIELECTRIC STACK BY ATOMIC LAYER DEPOSITION (ALD)

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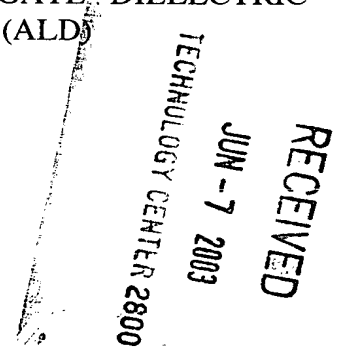

APPELLANT'S BRIEF ON APPEAL

(35 U.S.C. § 134(a) and 37 C.F.R. § 1.192(a))

Dear Sir:

This letter is Appellants' Brief on Appeal, under 35 U.S.C. § 134(a) and 37 C.F.R. § 1.192 (a), from the January 28, 2003, Final Rejection. This Appeal Brief is being filed in triplicate and is accompanied by the fee as set forth in 37 C.F.R. § 1.17(c).

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REAL PARTY IN INTEREST
(37 C.F.R. § 1.192(c)(1))

The real party in interest is the assignee of the patent application, Advanced Micro Devices, doing business at One AMD Place, M/S 68, Sunnyvale, CA, 94088-3453.

RELATED APPEALS AND INTERFERENCES
(37 C.F.R. § 1.192(c)(2))

On information and belief, no related appeals or interferences are pending.

STATUS OF CLAIMS
(37 C.F.R. § 1.192(c)(3))

Claims 1-3 and 5-19 are pending. Claims 4 and 20 have been cancelled. The final rejection of Claims 1-3 and 5-19 is herein appealed.

STATUS OF AMENDMENTS
(37 C.F.R. § 1.192(c)(4))

An Amendment in response to the Final Office Action was filed on March 18, 2003. The Examiner mailed an Advisory Action on May 21, 2003, therein indicating that the Amendment filed on March 18, 2003 had been entered.

SUMMARY OF INVENTION
(37 C.F.R. § 1.192(c)(5))

The present invention comprises a method for fabricating a semiconductor device having a gate insulator comprising a sandwich structure comprising a first ultra-thin nitride film, a layer of a high-k material, and a second ultra-thin nitride film, which sandwich

generally resides between a semiconductor substrate and a gate electrode. A substitute specification was filed on October 29, 2002, and references to page numbers and line numbers in the following description are with respect to the substitute specification.

Claim 1 recites a method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack. The method comprises initiating formation of the nitride/high-k material/nitride gate dielectric stack (page 4, lines 8, 9), depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an Atomic Layer Deposition (ALD) technique (page 4, lines 10-12), depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) (page 4, lines 12-15), and depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an Atomic Layer Deposition (ALD) technique (page 4, lines 16-19). The method of Claim 1 further includes completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure (page 4, lines 19-20), and completing fabrication of the device (page 4, line 25).

Claim 2 recites that the substrate of Claim 1 comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer (page 4, line 8).

Claim 3 recites that the first ultra-thin nitride film of Claim 1 comprises silicon nitride (Si_3N_4) (page 4, line 12), and that the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s) (page 4, line 11).

Claim 4 was cancelled.

Claim 5 recites that the thin metal film of Claim 1 further comprises tantalum (Ta) (page 4, line 12).

Claim 6 recites that the thin metal film of Claim 1 comprises a metal oxide (page 4, line 15).

Claim 7 recites that the second ultra-thin nitride film of Claim 1 comprises silicon nitride (Si_3N_4) (page 4, line 19), and that the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s) (page 4, line 18).

Claim 8 recites that completing formation of the nitride/high-k material/nitride gate

dielectric stack from the sandwich structure of Claim 1 comprises depositing a thick gate material on the second ultra-thin nitride film (page 4, 20-21), patterning the thick gate material, thereby forming a gate electrode (page 4, line 23) and etching portions of the sandwich structure uncovered by the gate electrode (page 4, line 24), thereby completing formation of the nitride/high-k material/nitride gate dielectric stack (page 4, lines 24-25).

Claim 9 recites that completing fabrication of the device of Claim 1 comprises forming of a MOSFET structure comprising the gate dielectric stack (page 4, line 26).

Claim 10 recites that the thick gate material of Claim 8 comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe) (page 4, lines 22-23), and wherein the thick gate material is patterned using a material such as photoresist (page 6, line 21).

Claim 11 recites that completing fabrication of the device of Claim 1 comprises forming a source/drain structure in the substrate and flanking the gate dielectric stack (page 4, lines 27-28), forming at least one spacer on at least one sidewall of the gate dielectric stack (page 4, line 28), and silicidizing a shallow source/drain region as well as the high-k gate stack (page 4, line 29), thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack (page 3, lines 29-30).

Claim 12 recites a method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising initiating formation of the nitride/high-k material/nitride gate dielectric stack (page 4, lines 8-9) by depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an Atomic Layer Deposition (ALD) technique (lines 4, 10-12), and wherein the substrate comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer (page 4, line 8), depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) (page 4, lines 12-15), and depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an Atomic Layer Deposition (ALD) technique (page 4, lines 16-19). The method of Claim 12 further includes completing formation of the nitride/high-k material/nitride gate dielectric stack from the

sandwich structure (page 4, lines 19-20), and completing fabrication of the device (page 4, line 25).

Claim 13 recites that the first ultra-thin nitride film of Claim 12 comprises silicon nitride (Si_3N_4) (page 4, line 12), and that the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s) (page 4, line 11).

Claim 14 depends from Claim 13 and recites that the thin metal film of Claim 12 further comprises tantalum (Ta) (page 4, lines 13-15), and wherein the thin metal film further comprises a metal oxide (page 4, line 15).

Claim 15 depends from Claim 14 and recites that the second ultra-thin nitride film of Claim 12 comprises silicon nitride (Si_3N_4) (page 4, line 19), and has a thickness in a range of 1 to 2 atomic layer(s) (page 4, line 18).

Claim 16 depends from Claim 15, and recites that the completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure of Claim 12 comprises depositing a thick gate material on the second ultra-thin nitride film (page 4, line 20-21), patterning the thick gate material, thereby forming a gate electrode (page 4, line 23), and etching portions of the sandwich structure uncovered by the gate electrode (page 4, line 24), thereby completing formation of the nitride/high-k material/nitride gate dielectric stack (page 4, lines 24-25).

Claim 17 depends from Claim 16, and recites that completing fabrication of the device of Claim 12 comprises forming of a MOSFET structure comprising the gate dielectric stack (page 4, line 26).

Claim 18 depends from Claim 17, and recites that the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe) (page 4, lines 22-23), and wherein the thick gate material is patterned using a material such as photoresist (page 6, line 21).

Claim 19 depends from Claim 18, and recites that completing fabrication of the device comprises forming a source/drain structure in the substrate and flanking the gate dielectric stack (page 4, lines 27-28), forming at least one spacer on at least one sidewall of the gate dielectric stack (page 4, line 28), and silicidizing a shallow source/drain region as well as the high-k gate stack (page 4, line 29), thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack (page 3,

lines 29-30).

Claim 20 was cancelled.

The claims on appeal are set forth in Appendix A.

ISSUE
(37 C.F.R. § 1.192(c)(6))

Whether Claims 1-3 and 5-19 are unpatentable under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

GROUPING OF CLAIMS
(37 C.F.R. § 1.192(c)(7))

Claims 2 and 5 - 12 stand or fall with Claim 1. Claims 13 and 14 stand or fall with Claim 3. Claims 16 - 19 stand or fall with Claim 15.

ARGUMENT
(37 C.F.R. § 1.192(c)(8))

On appeal, the Claims 1-3 and 5-19 have not been further amended since the March 18, 2003 Amendment, and are believed to have been placed in better form for this Appeal, notwithstanding the Appellants' belief that the claims would have been allowable as originally filed. All claims in this Appeal are believed to be fully supported by the Specification and are believed to be in allowable form. Favorable consideration of the present application is respectfully requested in light of these remarks, the following argument, the appendix, and the herewith submitted exhibits.

Issue 1: Whether the combination of Gardner et al. (US 5,963,810) and Dautartas et al. (US 6,124,158) was proper as a basis for a 35 U.S.C. § 103(a) rejection.

A. The Examiner's Argument for the Combination of Gardner and Dautartas.

The Examiner has rejected Claims 1-3 and 5-19 under 35 U.S.C. § 103(a) as being unpatentable under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158). In the Final Office Action mailed January 28, 2003, the Examiner proposed that Gardner disclosed the claimed invention except for using atomic layer deposition, and that Dautartus discloses "nitride films are deposited by using an Atomic Layer Deposition (ALD) technique (col. 1, lns. 15-30). The Examiner further stated that:

> "... it would have been obvious to one of ordinary skill in the art at the time of the invention to form nitride layers using an ALD technique, because this deposition technique provides excellent uniformity and surface conformity of thin insulator films"

B. Analysis

However, the Examiner has not shown how Gardner or Dautartus motivate their combination to form the present invention, and therefore not established a prima facie case of obviousness. The Manual for Patent Examiners' Practice paragraph 2142 addresses the requirements for a prima facie case of obviousness, stating that ". . .To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), MPEP Section 706.02(j). **"Mere fact that prior art may be modified to reflect features of claimed invention does not make modification, and hence claimed invention, obvious unless desirability of such modification is suggested by prior art. . .",** *In re Fritch*, 922 F.2d 1260, 23 USPQ.2d 1780, at p. 1780 (Fed. Cir. 1992). Thus, either a single reference including all the limitations of the claim, or motivation to combine references collectively including all the limitations of the claim, are required to establish a *prima facie* case of obviousness.

Gardner was cited in the Office Action as providing depositing a first nitride film,

depositing a high-k dielectric material, depositing a second nitride film, and completing the fabrication of the device. The Office Action states that one skilled in the art would have combined atomic layer deposition taught in Dautartas with Gardner because this deposition technique provides excellent uniformity and surface conformity of thin insulator films . However, merely pointing out that the result of a combination has an advantage is not sufficient to establish that the combination is obvious, and is inconsistent with the requirement that an invention has utility. Establishment of a *prima facie* case of obviousness requires showing that the combination is suggested or motivated by the reference. The Office Action has failed to show that Gardner or Dautartas suggest or motivate their combination, and therefore a *prima facie* case of obviousness has not been established.

Further, in the embodiment of Gardener cited by the Examiner, Gardner specifically teaches deposition of both a nitride layer and a high permittivity gate insulating layer by sputter deposition using the same reaction chamber (col. 2, lns. 37-40). The suggestion by the Examiner to replace sputter deposition of the nitride layer in Gardner, with the atomic layer deposition of the nitride layer taught by Dautartas, is not consistent with the use of a single chamber recited in Gardner.

Gardner also recites a nitride thickness of 5 to 15 Å achieved by sputtering (col. 5, ln. 49), while Dautartas teaches tens or hundreds of atomic layers formed by atomic layer deposition (col. 3, lns. 49-50). Each cycle of an atomic layer deposition deposits one atomic layer. An atomic layer of, for example silicon nitride, is the thickness of a silicon nitride molecule, or about 3.5 Å. Thus, the thickness of tens of layers of silicon nitride is 35 Å, or more. Therefore, substitution of the tens to hundreds of nitride layers formed by atomic layer deposition described in Dautartas, for the 5 to 15 Å achieved by sputtering in Gardner, is not consistent with the teaching of Gardner, and does not achieve Gardner's goal of minimizing the nitride layer (col. 5, lns. 45-46). Further, the Examiner has presented no reference teaching a layer deposited by ALD which is 1 to 2 atomic layers thick.

C. Conclusion

Because the Examiner has not shown that the references suggest their combination, and because Gardner teaches deposition of the nitride layer and the high-k layer in a single

chamber versus two separate processes of atomic layer deposition for the nitride layer and sputtering for the high-k layer, and because Gardner teaches a 5 to 15 Å nitride layer, and Dautartas teaches a layer at least 35 Å thick, there is no motivation for the combination of these references. Therefore, the Applicant believes that the Examiner's combination of these reference is erroneous and request that the rejections of Claims 1-3 and 5-19, which rejections require the combination of the Gardner and Dautartas, be reversed.

Issue 2: Whether Claim 1 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

A. The Examiner's Argument for the rejection of Claim 1.

The Examiner proposed that Gardner discloses depositing a first nitride film, depositing a high-k material, depositing a second nitride film, and completing fabrication of the device. The Examiner further proposed that Dautartas discloses deposition of the nitride films by atomic layer deposition.

B. Analysis

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 1 includes a limitation of:

> depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti)

In the Advisory Action mailed May 21, 2003, the Examiner upheld the rejection of Claims 1-3 and 5-19, stating that:

> The request for reconsideration has been considered but does not place the application in condition for allowance because: In the after final amendment the Applicant adds the particular materials from the group of materials that were disclosed in a dependent claim into the independent claims. However, this amendment does not overcome the final rejection because Applicant has not shown that a different result would be gained by using one of the materials of the group versus the others. Especially since the various materials listed are transition metal and have similar properties. Also, on page 3 lines 1-8 of the Applicant's specification states that formation of all the disclosed metal insulators is known in the art.

Although the Examiner correctly pointed out that Claim 1 includes a group consisting of all but one material described in the specification, this is not a valid grounds for rejection of Claim 1. MPEP paragraph 2144.06 "Art Recognized Equivalence for the Same Purpose" states:

> In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency must be recognized in the prior art, and **cannot be based on applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents**. In re Ruff, 256 F.2d 590, 118 USPQ 340 (CCPA 1958) (The mere fact that components are claimed as members of a Markush group cannot be relied upon to establish the equivalency of these components. However, an applicant's expressed recognition of an art-recognized or obvious equivalent may be used to refute an argument that such equivalency does not exist.)

The Examiner has relied upon the specification of the present invention to establish equivalence and reject Claim 1. Because the equivalence is not based on prior art, the Applicant believes that equivalence has not been established in accordance with MPEP paragraph 2144.06, and that the rejection is erroneous.

C. Conclusion

Because sufficient grounds for combination of the references have not been presented, and because the basis for rejection enunciated in the Advisory Action is not in accord with the MPEP or case law, the Applicant believes that Claim 1 is in condition for allowance. Therefore, the Applicants request that the rejection of Claim 1 be reversed.

Issue 3: Whether Claim 2 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 2 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 2 stands or falls with Claim 1.

Issue 4: Whether Claim 3 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

The Applicant believes that Claim 3 includes an independently patentable limitation and that as a result, Claim 3 stands or falls alone.

A. The Examiner's Argument for the rejection of Claim 3.

The Examiner argued that Claim 3 is obvious over Gardner in view of Dautartas because Dautartas suggests the use of silicon nitride as a nitride film.

B. Analysis

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 3 includes a limitation that:

the first ultra-thin nitride film has a thickness in a range of **1 or 2 atomic layers**

Therefore, even if Gardner are Dautartas are combined, Dautartas teaches the deposition of silicon nitride of **tens to hundreds of atomic layers**. Because the silicon nitride film taught by Dautartas is orders of magnitude thicker than the first silicon nitride film of the present invention, the combination of Gardner and Dautartas does not provide a 1 to 2 atomic layer thick layer of silicon nitride.

C. **Conclusion**

Because sufficient grounds for combination of the references have not been presented, and because even if combined, the Dautartas does not teach the 1 to 2 atomic layer thick first silicon nitride layer of the present invention, the Applicant believes that the rejection of Claim 3 is erroneous and request that the rejection of Claim 3 be reversed.

Issue 5: Whether Claim 5 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 5 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 5 stands or falls with Claim 1.

Issue 6: Whether Claim 6 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 6 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 6 stands or falls with Claim 1.

Issue 7: Whether Claim 7 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

The Applicant believes that Claim 7 includes an independently patentable limitation and that as a result, Claim 7 stands or falls alone.

A. The Examiner's Argument for the rejection of Claim 7.

The Examiner argued that Claim 7 is obvious over Gardner in view of Dautartas because Dautartas suggests the use of silicon nitride as a second nitride film.

B. **Analysis**

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 7 includes a limitation that:

the second ultra-thin nitride film has a thickness in a range of **1 or 2 atomic layers**

Therefore, even if Gardner are Dautartas are combined, Dautartas teaches the deposition of silicon nitride of **tens to hundreds of atomic layers**. Because the silicon nitride film taught by Dautartas is orders of magnitude thicker than the silicon nitride film of the present invention, the combination of Gardner and Dautartas does not provide a 1 to 2 atomic layer thick second layer of silicon nitride.

C. **Conclusion**

Because sufficient grounds for combination of the references have not been presented, and because even if combined, the Dautartas does not teach the second 1 to 2 atomic layer thick silicon nitride layer of the present invention, the Applicant believes that the rejection of Claim 7 is erroneous and request that the rejection of Claim 7 be reversed.

Issue 8: Whether Claim 8 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 8 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 8 stands or falls with Claim 1.

Issue 9: Whether Claim 9 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 9 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 9 stands or falls with Claim 1.

Issue 10: Whether Claim 10 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 10 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 10 stands or falls with Claim 1.

Issue 11: Whether Claim 11 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 11 depends upon Claim 1 which the Applicant believes to be in condition for allowance. As such, Claim 11 stands or falls with Claim 1.

Issue 12: Whether Claim 12 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

A. The Examiner's Argument for the rejection of Claim 12.

The Examiner proposed that Gardner discloses depositing a first nitride film, depositing a high-k material, depositing a second nitride film, and completing fabrication of the device. The Examiner further proposed that Dautartas discloses deposition of the nitride films by atomic layer deposition.

B. Analysis

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 1 includes a limitation of:

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti)

In the Advisory Action mailed May 21, 2003, the Examiner upheld the rejection of Claims 1-3 and 5-19, stating that:

The request for reconsideration has been considered but does not place the application in condition for allowance because: In the after final amendment the Applicant adds the particular materials from the group of materials that were disclosed in a dependent claim into the independent claims. However, this amendment does not overcome the final rejection because Applicant has not shown that a different result would be gained by using one of the materials of the group versus the others. Especially since the various materials listed are transition metal and have similar properties. Also, on page 3 lines 1-8 of the Applicant's specification states that formation of all the disclosed metal insulators is known in the art.

Although the Examiner correctly pointed out that Claim 12 includes a group consisting of all but one material described in the specification, this is not a valid grounds for rejection of Claim 12. MPEP paragraph 2144.06 "Art Recognized Equivalence for the Same Purpose" states:

In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency must be recognized in the prior art, and **cannot be based on applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents**. In re Ruff, 256 F.2d 590, 118 USPQ 340 (CCPA 1958) (The mere fact that components are claimed as members of a Markush group cannot be relied upon to establish the equivalency of these components. However, an applicant's expressed recognition of an art-recognized or obvious equivalent may be used to refute an argument that such equivalency does not exist.)

The Examiner has relied upon the specification of the present invention to establish equivalence and reject Claim 12. Because the equivalence is not based on prior art, the Applicant believes that equivalence has not been established in accordance with MPEP paragraph 2144.06, and that the rejection is erroneous.

C. Conclusion

Because sufficient grounds for combination of the references have not been presented, and because the basis for rejection enunciated in the Advisory Action is not in accord with the MPEP or case law, the Applicant believes that Claim 12 is in condition for allowance. Therefore, the Applicants request that the rejection of Claim 12 be reversed.

Claim 12 includes the same patentably distinct limitations that are present in Claim 1. As such, Claim 12 stands or falls with Claim 1.

Issue 13: Whether Claim 13 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

A. The Examiner's Argument for the rejection of Claim 13.

The Examiner argued that Claim 13 is obvious over Gardner in view of Dautartas because Dautartas suggests the use of silicon nitride as a nitride film.

B. Analysis

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 13 includes a limitation that:

the first ultra-thin nitride film has a thickness in a range of **1 or 2 atomic layers**

Therefore, even if Gardner are Dautartas are combined, Dautartas teaches the deposition of silicon nitride of **tens to hundreds of atomic layers**. Because the silicon nitride film taught by Dautartas is orders of magnitude thicker than the first silicon nitride film of the present invention, the combination of Gardner and Dautartas does not provide a 1 to 2 atomic

layer thick layer of silicon nitride.

C. Conclusion

Because sufficient grounds for combination of the references have not been presented, and because even if combined, the Dautartas does not teach the 1 to 2 atomic layer thick first silicon nitride layer of the present invention, the Applicant believes that the rejection of Claim 13 is erroneous and request that the rejection of Claim 13 be reversed.

Claim 13 includes the same patentably distinct limitations that are present in Claim 3. As such, Claim 13 stands or falls with Claim 3.

Issue 14: Whether Claim 14 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 14 depends upon Claim 13 which the Applicant believes to be in condition for allowance. As such, Claim 14 stands or falls with Claim 13.

Issue 15: Whether Claim 15 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

The Applicant believes that Claim 15 includes an independently patentable limitation and that as a result, Claim 15 stands or falls alone.

A. The Examiner's Argument for the rejection of Claim 15.

The Examiner argued that Claim 15 is obvious over Gardner in view of Dautartas because Dautartas suggests the use of silicon nitride as a nitride film.

B. Analysis

As described for issue 1 above, the Applicant believes that a prima facie case of obviousness has not been established because sufficient grounds for the combination of Gardner and Dautartas is not present.

Further, Claim 15 depends from Claim 13 through Claim 14, and thus includes limitations that:

> the first ultra-thin nitride film has a thickness in a range of **1 or 2 atomic layers**; and
> the second ultra-thin nitride film has a thickness in a range of **1 or 2 atomic layers**

Therefore, even if Gardner and Dautartas are combined, Dautartas teaches the deposition of silicon nitride of **tens to hundreds of atomic layers**, not the one to two layers of the present invention. Because the silicon nitride film taught by Dautartas is orders of magnitude thicker than the first and second silicon nitride films of the present invention, the combination of Gardner and Dautartas does not provide the one to two atomic layer thick layers of silicon nitride described in Claim 15.

C. Conclusion

Because sufficient grounds for combination of the references have not been presented, and because even if combined, the Dautartas does not teach the 1 to 2 atomic layer thick first and second silicon nitride layers of the present invention, the Applicant believes that the rejection of Claim 15 is erroneous and request that the rejection of Claim 15 be reversed.

Issue 16: Whether Claim 16 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 16 depends upon Claim 15 which the Applicant believes to be in condition for allowance. As such, Claim 16 stands or falls with Claim 15.

Issue 17: Whether Claim 17 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 17 depends upon Claim 16 which the Applicant believes to be in condition for allowance. As such, Claim 17 stands or falls with Claim 15.

Issue 18: Whether Claim 18 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 18 depends upon Claim 17 which the Applicant believes to be in condition for allowance. As such, Claim 18 stands or falls with Claim 15.

Issue 19: Whether Claim 19 is Unpatentable Under 35 U.S.C. § 103(a) over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158).

Claim 19 depends upon Claim 18 which the Applicant believes to be in condition for allowance. As such, Claim 19 stands or falls with Claim 15.

CONCLUSION

For the forgoing reasons, the Applicant respectfully submits that Gardner and Dautartas were improperly combined as 35 U.S.C. § 103(a) references, and further submit that the rejections of Claims 1-3 and 5-19 in the Advisory Action were improperly based on an argument that the Applicant was required to show that a different result would be gained by using one of the materials in a group versus the others. Accordingly, reconsideration of the present application in light of the these remarks is respectfully requested. In view of the foregoing arguments, the Appellants respectfully request that the rejection of Claims 1-3 and 5-19 be REVERSED.

Respectfully submitted,

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APPENDIX A:
CLAIMS ON APPEAL (37 C.F.R. § 1.192(c)(9))

Claims:

1. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

2. A method as recited in claim 1, wherein the substrate comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer.

3. A method as recited in claim 1, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

4. **(canceled)**

5. A method as recited in claim 1, wherein the thin metal film further comprises tantalum (Ta).

6. A method as recited in claim 1, wherein the thin metal film comprises a metal oxide.

7. A method as recited in claim 1, wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

8. A method as recited in claim 1, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

depositing a thick gate material on the second ultra-thin nitride film;

patterning the thick gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

9. A method as recited in claim 1, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

10. A method as recited in claim 8, wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and wherein the thick gate material is patterned using a material such as photoresist.

11. A method as recited in claim 1, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby

forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

12. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and wherein the substrate comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

13. A method as recited in claim 12, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

14. A method as recited in claim 13, wherein the thin metal film further comprises tantalum (Ta), and wherein the thin metal film further comprises a metal oxide.

15. A method as recited in claim 14, wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

16. A method as recited in claim 15, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

depositing a thick gate material on the second ultra-thin nitride film;

patterning the thick gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

17. A method as recited in claim 16, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

18. A method as recited in claim 17, wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and wherein the thick gate material is patterned using a material such as photoresist.

19. A method as recited in claim 18, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

20. **(canceled)**

Exhibit A: Present Invention (US 09/826,472)

PATENT
Docket No. P1296

TITLE OF THE INVENTION

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A NITRIDE/HIGH-K/NITRIDE GATE DIELECTRIC STACK BY ATOMIC LAYER DEPOSITION (ALD)

CROSS-REFERENCE TO RELATED APPLICATION(S)

Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

REFERENCE TO A MICROFICHE APPENDIX

Not Applicable

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to semiconductor devices and their methods of fabrication. More particularly, the present invention relates to the formation of gate stacks. Even more particularly, the present invention relates to forming a gate stack having superior thermal stability and reduced diffusion into silicon-bearing semiconductor structures.

2. Description of the Background Art

[0002] Currently, the semiconductor industry has an interest in reducing the critical dimensions of transistors. As such, the thickness of the gate oxide must also be reduced. In so doing, the

related art has faced problems associated with a significant increase in direct tunneling leakage current through a very thin gate oxide (i.e., < 25 Angstroms). In an effort to suppress the severe gate leakage current, a high dielectric constant (high-k) material may be used as a gate dielectric, replacing a conventional thermal oxide. Several high dielectric constant (high-k) materials (metal oxides) are good candidates for gate dielectric insulators: zirconia or zirconium dioxide (ZrO_2), hafnia or hafnium dioxide (HfO_2), titania or titanium dioxide (TiO_2), tantala or tantalum pentoxide (Ta_2O_5), and the like.

[0003] However, a high-k gate dielectric insulator, such as the foregoing metal oxides, must have a thickness which is much greater than that of a conventional thermal oxide to be similarly effective, because the direct current density is exponentially proportional to a dielectric layer's thickness. Thus, the direct tunneling current flow through a gate dielectric insulator may be significantly reduced, motivating its use in very small transistors. Another major problem with using a high-k material is thermal instability. High-k materials tend to diffuse into the silicon (Si) substrate, a polysilicon (poly-Si) gate, or a polysilicon-germanium (poly-SiGe) gate during subsequent high temperature processing steps. Therefore, a need exists for a method of fabricating a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into the Si substrate, the poly-Si gate, or the poly-SiGe gate when experiencing subsequent high temperature processes.

BRIEF SUMMARY OF THE INVENTION

[0004] Accordingly, the present invention provides a method of fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, and a device thereby formed. Generally, the present invention device has a high-k gate dielectric insulator (i.e., a nitride/high-k material/nitride gate dielectric stack) formed by atomic layer deposition (ALD). The present invention method for fabricating the present device, generally comprises: depositing a first ultra-thin nitride film; depositing a high-k material film; and depositing a second ultra-thin nitride film. The unique features of the present method basically involve a sandwich structure formed by depositing an ultra-thin nitride film, which may comprise silicon nitride (Si_3N_4), before and after depositing the high-k material film, which may comprise a thin metal film, whereby the first ultra-thin nitride film provides resistance

to metal diffusion into the Si substrate, the poly-Si gate electrode, or the poly-SiGe gate electrode. This present invention device, so formed, has the advantages of providing sufficient diffusion resistance as well as thermal stability in a thin (i.e., small) feature size.

[0005] By way of example, and not of limitation, a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, may be fabricated according to the present invention by: (a) providing a substrate, wherein the substrate may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer; (b) initiating formation of a nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on the substrate, wherein the first ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the first ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (c) depositing a high-k material, which may comprise a thin metal film, on the first ultra-thin nitride film, wherein the thin metal film may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film may also comprise a metal oxide; (d) depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the second ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (e) completing formation of the nitride/high-k material/nitride gate dielectric stack, wherein the step (e) comprises (e)(1) depositing a thick gate material on the second ultra-thin nitride film, wherein the thick gate material may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); (e)(2) patterning the thick gate material, thereby forming a gate electrode; and (e)(3) etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the stack; and (f) completing fabrication of the semiconductor device, wherein step (f) may comprise the forming of a MOSFET structure comprising the stack, wherein the step (f) may further comprise (f)(1) forming a source/drain structure in the substrate and flanking the stack, (f)(2) forming at least one spacer on at least one sidewall of the stack, and (f)(3) silicidizing a shallow source/drain region of the substrate as well as the stack, thereby respectively forming a source/drain silicide in the shallow region and a gate silicide on the stack.

[0006] Advantages of the present invention include the reduction of direct tunneling current flow through a gate dielectric insulator of a semiconductor device, and the fabrication of a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes. Further advantages of the invention will be demonstrated in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without thereon placing limitations.

BRIEF DESCRIPTION OF THE DRAWING

[0007] For a better understanding of the present invention, reference is made to the several figures of the below-referenced accompanying Drawing which is illustrative in purpose and where like reference numbers denote like elements.

[0008] FIG. 1 through FIG. 6, together, constitute a process flow diagram of the fabrication of a semiconductor device, in accordance with the present invention, wherein the semiconductor device is shown in cross-section at various stages of the process.

DETAILED DESCRIPTION OF THE INVENTION

[0009] Referring more specifically to the drawings for illustrative purposes, the present invention is embodied in the apparatus and method generally shown in FIG. 1 through FIG. 6. These figures depict an embodiment of a process for fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes. Each figure illustrates a particular processing stage, and presents a side view in cross-section of the device at that stage of processing. However, that the apparatus may vary as to configuration and as to details of the parts, and that the method may vary as to the specific steps and sequence, without departing from the basic concepts as disclosed herein, will be appreciated.

[0010] Referring first to Figure 1, in the first stage of processing, a substrate 10 is provided, wherein the substrate 10 may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer.

[0011] Next, as shown in Figure 2, a first ultra-thin nitride film 21 is deposited on the substrate 10, thereby initiating formation of a nitride/high-k material/nitride gate dielectric stack, wherein the first ultra-thin nitride film 21 may be deposited using an atomic layer deposition (ALD) technique, wherein the first ultra-thin nitride film 21 may comprise silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film 21 may be a thickness in a range of 1 - 2 atomic layer(s).

[0012] Next, as shown in Figure 3, a high-k material, such as a thin metal film 30, is deposited on the first ultra-thin nitride film 21, wherein the thin metal film 30 may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film 30 also comprises a metal oxide.

[0013] Next, as shown in Figure 4, a second ultra-thin nitride film 22 is deposited on the high-k material (e.g., the thin metal film 30), thereby forming a sandwich structure 35, wherein the second ultra-thin nitride film 22 may be deposited using an atomic layer deposition (ALD) technique, and wherein the second ultra-thin nitride film 22 may comprise silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film 22 may have a thickness in a range of 1 - 2 atomic layer(s).

[0014] Next, as shown in Figure 5, a completed nitride/high-k material/nitride gate dielectric stack 40 is formed on the substrate 10, wherein the stack 40 is completed by depositing a thick gate material 31 on the second ultra-thin nitride film 22, wherein the thick gate material 31 may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); patterning the thick gate material 31 with a material such as a photoresist (not shown), thereby forming a gate electrode 32; and etching portions of the sandwich structure 35 uncovered by the gate electrode 32, thereby forming the nitride/high-k material/nitride gate dielectric stack 40.

[0015] As depicted in Figure 6, a MOSFET structure 50 comprises the stack 40, wherein the MOSFET structure 50 further comprises a source/drain structure 51 formed in the substrate 10 and flanking the stack 40, at least one spacer 52 formed on at least one sidewall of the stack 40, and a shallow source/drain region 15 as well as the nitride/high-k/nitride gate dielectric stack 40 being silicidized to respectively form a source/drain silicide 16 in the shallow region 15 of the substrate 10 and a gate silicide 41 on the stack 40.

[0016] Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

[0017] Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. §112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

CLAIMS

What is claimed:

1. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

2. A method as recited in claim 1, wherein the substrate comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer.

3. A method as recited in claim 1, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

4. **(canceled)**

5. A method as recited in claim 1, wherein the thin metal film further comprises tantalum (Ta).

6. A method as recited in claim 1, wherein the thin metal film comprises a metal oxide.

7. A method as recited in claim 1, wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

8. A method as recited in claim 1, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

depositing a thick gate material on the second ultra-thin nitride film;

patterning the thick gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

9. A method as recited in claim 1, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

10. A method as recited in claim 8, wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and wherein the thick gate material is patterned using a material such as photoresist.

11. A method as recited in claim 1, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

12. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein

the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and wherein the substrate comprises a material selected from a group consisting of a silicon wafer and a silicon-on-insulator (SOI) wafer;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

13. A method as recited in claim 12, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

14. A method as recited in claim 13, wherein the thin metal film further comprises tantalum (Ta), and wherein the thin metal film further comprises a metal oxide.

15. A method as recited in claim 14, wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

16. A method as recited in claim 15, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

depositing a thick gate material on the second ultra-thin nitride film;

patterning the thick gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

17. A method as recited in claim 16, wherein completing fabrication of the device

comprises forming of a MOSFET structure comprising the gate dielectric stack.

18. A method as recited in claim 17, wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and wherein the thick gate material is patterned using a material such as photoresist.

19. A method as recited in claim 18, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

20. **(canceled)**

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING NITRIDE/HIGH-K/NITRIDE GATE DIELECTRIC STACK BY ATOMIC LAYER DEPOSITION (ALD) AND SEMICONDUCTOR DEVICE THEREBY FORMED

ABSTRACT

A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack with good thermal stability which does not diffuse into a silicon substrate, a polysilicon gate, or a polysilicon-germanium gate when experiencing subsequent high temperature processes, comprising the steps of: (a) providing a substrate; (b) initiating formation of the nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on the substrate; (c) depositing a high-k material, such as a thin metal film, on the first ultra-thin nitride film; (d) depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure; (e) completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and (f) completing fabrication of the semiconductor device, and a device thereby formed.